A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier

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***Abstract*—A fully integrated 1.9-GHz CMOS low-noise amplifier (LNA) has been implemented in a 0.8-μm CMOS technology. For low-noise performance, the amplifier employs high-quality spiral inductors with a quality factor of 8.5–12.5, and device layout and bias condition of the active devices were optimized for low-noise conditions. This amplifier showed a noise figure of 2.8 dB with a forward gain of 15 dB at current consumption of 15 mA. To the authors' knowledge, this represents the lowest noise figure reported to date for a fully integrated CMOS LNA operating at 1.9 GHz.**

***Index Terms*— CMOS LNA, fully integrated amplifier, low noise.**

I. Introduction

THE strong demand for portable wireless communication systems motivates the research of radio frequency (RF) modules using CMOS technology. The use of CMOS technology is very attractive for the integrating the baseband intermediate frequency (IF) and RF modules in a single chip. Recently, RF receivers for 1.9 GHz have been implemented by submicron CMOS technology [1]–[5]. Since the noise performance of the fully integrated CMOS low-noise amplifier (LNA) is poor, most of the reported LNA circuits use high-quality off-chip inductors that include bonding wires to prevent any further degradation of noise performance. However, using bonding wire as an inductor has a drawback of repeatability. The noise performance of a monolithic LNA depends on the circuit topology, the minimum noise figure ($F_{\min}$) of the active device, and the quality factor (Q) of spiral inductors. The major cause of poor noise performance in fully integrated LNA's is due to the low quality of on-chip spiral inductors.

In this letter, we demonstrate a fully integrated, very low-noise 1.9-GHz CMOS LNA employing high-Q inductors and optimized active devices. The measured the noise performance of the amplifier agrees well with the simulation using the parameters obtained from the active device and high-Q spiral inductors.

II. LNA Design

A schematic of the two-stage LNA is shown in Fig. 1. The first stage of the circuit employs a common source with inductive source degeneration type for simultaneous matching of noise and power gain [3]–[5]. The transistor M_1 with the channel width of 600 μm was selected for low $F_{\min}$ and convenience in matching [6]. Our 0.8-μm n-MOSFET with the channel width of 600 μm has a $F_{\min}$ of 1.0 dB at drain current of 5 mA [6]. The bias condition of the second-stage transistor M_2 was chosen for the high gain and linearity. Transistors M_3 and M_4 with 10-kΩ resistor R_b for ac blocking forms the biasing circuitry. The 6.8-nH inductor Lg and 9-nH inductor Lo are used for input and output matching, respectively. The inductors with a thick metal (3.1 μm) have a Q value of 12.5 and an inductance of 9 nH as shown in Fig. 2 [7], [8].

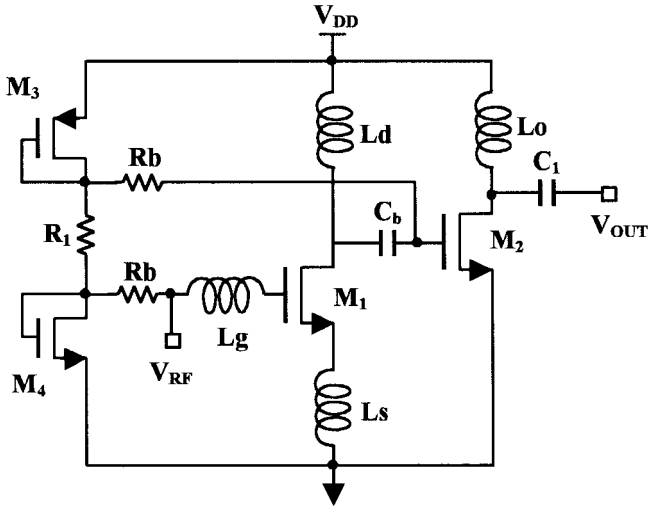

Fig. 1. Simplified schematic of the fully integrated LNA.

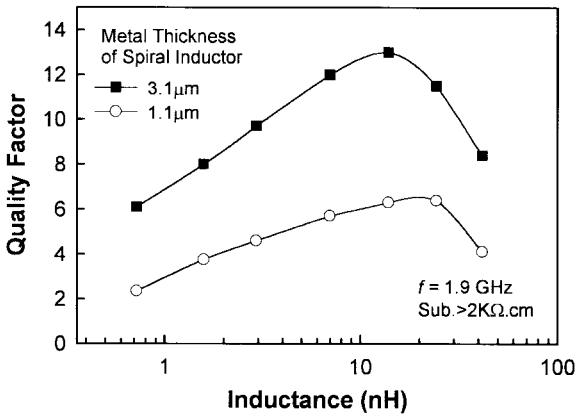

Fig. 2. Quality factor versus inductance of spiral inductors fabricated with standard (1.1 μm) process and thick (3.1 μm) metal process.

Manuscript received April 21, 1998. This work was supported by the Ministry of Informations and Communication, Korea.

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Publisher Item Identifier S 1051-8207(98)05620-7.

TABLE I
COMPARISON OF 1.6–1.9-GHz CMOS LNA PERFORMANCE REPORTED IN THE LITERATURE

Author	*freq.*	Gain	NF	Current	Input Matching	Technology	Ref.
Shaeffer *et al.*	1.6 GHz	22 dB	2.4 dB	5 mA	Wire+on chip	0.5 μm	[1]
Wu *et al.*	1.8 GHz	20 dB	-	5 mA	Off chip	0.6 μm	[2]
Shahani *et al.*	1.6 GHz	17 dB	3.8 dB	8 mA	On chip	0.35 μm	[3]
Rudel *et al.*	1.9 GHz	22 dB	5.0 dB	12 mA	Wire+on chip	0.6 μm	[4]
Shaeffer *et al.*	1.6 GHz	22 dB	3.5 dB	20 mA	Wire+on chip	0.6 μm	[5]
This work	1.9 GHz	15 dB	2.8 dB	15 mA	On chip	0.8 μm	-

The LNA was simulated with linear simulator using the measured S- and noise parameter data for the active devices, and the lumped small signal equivalent circuit parameter of high-Q spiral inductors.

III. EXPERIMENTAL RESULTS

The LNA circuit was fabricated using 0.8-μm standard CMOS technology fabricated on high-resistivity silicon substrate (>2 kΩ·cm). The second metal thickness was increased to 3.1 μm to reduce the series resistance of spiral inductors. All the measurements were carried out using on-wafer RF probes and a HP8510C Network Analyzer. Noise parameters were also measured over the frequency range of 0.3–3 GHz using an ATN setup.

The microphotograph of a monolithic LNA fabricated using the thick metal process is shown in Fig. 3. The chip size was 0.93 mm × 0.93 mm. Fig. 4 shows the measured results of gain and S_{11} of the amplifier, which show good agreement with the simulated ones. The amplifier has a gain of 15 dB, a S_{11} of −16.4 dB, and S_{22} of −7 dB at 1.9 GHz. It consumes dc current of 15 mA including bias circuit from a 3.6-V supply.

Fig. 5 compares the measured noise figure of the LNA's fabricated with standard thin- and thick-metal process. The second metal thickness of the standard and thick-metal CMOS process was 1.1 and 3.1 μm, respectively. The circuit fabricated using thick-metal process shows the noise figure of 2.8 dB at 1.9 GHz. The performance of L-band CMOS LNA's reported in the literature is listed in Table I. Compared to other CMOS LNA's that usually use the off-chip [2], [5] or bonding wire inductor [1], [4] as input-matching element, this monolithic 1.9-GHz LNA circuit shows the lowest noise figure. Furthermore, Fig. 5 shows that an amplifier employing thick-metal inductors can improve the noise figure up to 1.0 dB and gain by 2.0 dB compared with the one fabricated with the standard thin-metal CMOS process. The noise performance of the LNA's can be expected accurately by the simulation using small-signal parameters of active and passive devices.

The amplifier has a measured −1-dB input compression point of −10 dBm, and the measured third-order intermodulation intercept point was 2 dBm referred at the input.

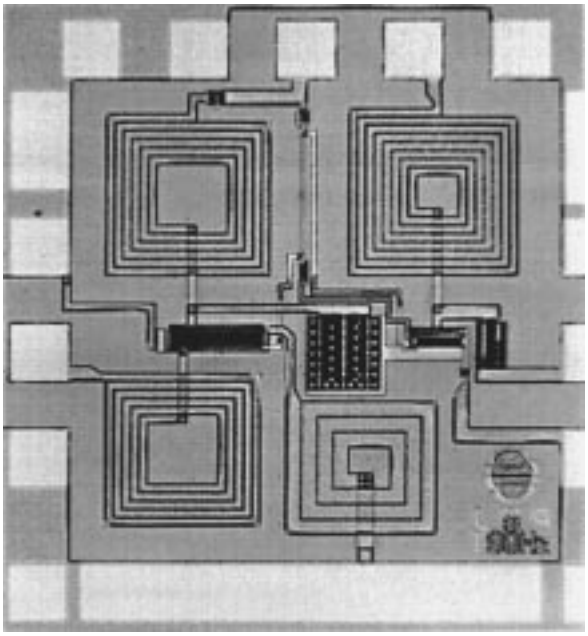

Fig. 3. Microphotograph of CMOS LNA fabricated with thick metal process. The four inductors and bias circuit were also integrated in a chip that has the size of 0.93 mm × 0.93 mm.

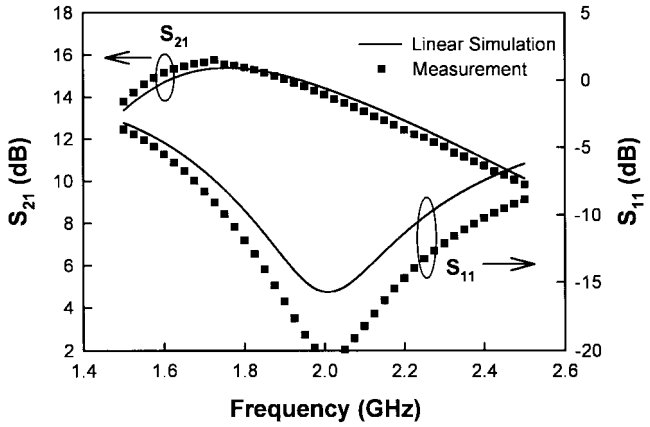

Fig. 4. Measured versus simulated gain and S_{11} of the proposed LNA. The maximum gain peak obtained at 1.7 GHz, because the amplfier has the minimum S_{22} at 1.65 GHz with the value of −18 dB.

IV. CONCLUSIONS

A fully integrated 1.9-GHz CMOS LNA with high-Q inductors has been designed and fabricated using a 0.8-μm CMOS technology on high-resistivity silicon substrate with the thick metal process. The measured noise figure and gain at a supply voltage of 3.6 V are 2.8 and 15 dB, respectively, which agrees

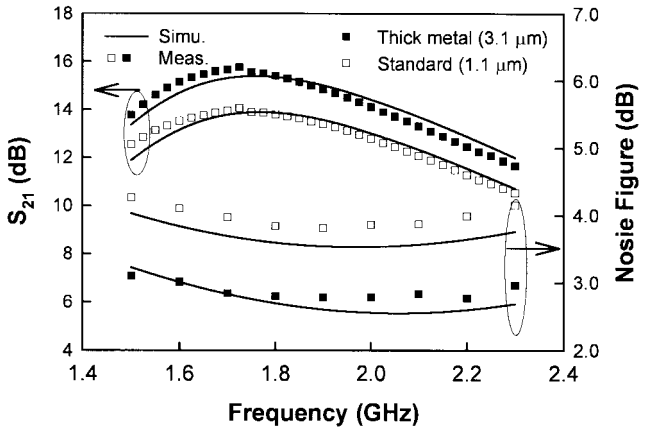

Fig. 5. Comparison between measured and simulated gain and the noise figure of LNA's fabricated with standard thin and thick metal process.

well with the simulation results calculated using small-signal parameters obtained separately from the active and the passive devices.

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